What is claimed is:

DEVICE FOR USE IN CONTROLLING A SAMPLE RATE

1. A communication circuit comprising:

an all-digital loop circuit to control a clock rate of a digital circuit element to be a function of a frequency of a signal received by the communication circuit.

2. The communication circuit claimed in claim 1 wherein the communication circuit further includes an analog-to-digital converter, coupled to the loop circuit, that digitizes the signal received.

3. The communication circuit claimed in claim 2 wherein the digital circuit element includes a digital decimation filter, coupled to the analog-to-digital converter.

4. The communication circuit claimed in claim 3 wherein the analog-to-digital converter operates at a fixed clock rate and the decimation filter operates at a variable clock rate.

5. The communication circuit claimed in claim 4 wherein digital loop circuit provides a digital signal to control the clock rate.

6. A circuit comprising:

a loop circuit to control a sample rate of a digital circuit element.

7. The circuit of claim 6 wherein the loop circuit comprises a digital loop circuit.

8. The circuit of claim 6 wherein the digital circuit element receives an input sampled data stream and provides an output sampled data stream, and wherein the loop circuit controls the sample rate of the output data stream.

9. The circuit of claim 7 wherein the digital loop circuit controls the sample rate of the digital circuit element to be a function of a frequency of a signal received by the circuit.

10. The circuit claimed in claim 9 wherein the circuit further includes an analog-to-digital converter, coupled to the loop circuit, that digitizes the signal received.

11. The circuit claimed in claim 10 wherein the digital circuit element includes a digital decimation filter, coupled to the analog-to-digital converter.

12. The circuit claimed in claim 11 wherein the analog-to-digital converter operates at a fixed clock rate and the decimation filter operates at a variable clock rate.

13. The circuit claimed in claim 12 wherein digital loop circuit provides a digital signal to control the clock rate.

14. The circuit of claim 9 wherein the circuit comprises a communication circuit.

15. The communication circuit claimed in claim 14 wherein the communication circuit further includes an analog-to-digital converter, coupled to the loop circuit, that digitizes the signal received.

16. The communication circuit claimed in claim 15 wherein the digital circuit element includes a digital decimation filter, coupled to the analog-to-digital converter.

17. The communication circuit claimed in claim 16 wherein the analog-to-digital converter operates at a fixed clock rate and the decimation filter operates at a variable clock rate.

18. The communication circuit claimed in claim 17 wherein digital loop circuit provides a digital signal to control the clock rate.

19. A device that receives two or more sampled data streams having sample rates different from one another, converts the sample rate of one or more of the data streams to provide two or more data streams having sample rates compatible with one another, and combines the two data streams.

20. The device of claim 14 wherein the device converts the sample rate of one or more of the data streams to provide two or more data streams having sample rates that are integer multiples of one another, and combines the two data streams.

21. The device of claim 14 wherein the device converts the sample rate of one or more of the data streams to provide two or more data streams having sample rates that are equal to one another, and combines the two data streams.

22. A clock recovery circuit comprising a sample rate converter.

23. A phase locked loop comprising a sample rate converter.

24. A device comprising:

at least one sample rate converter that receives a sampled data stream and outputs two separate data streams having output sample rates that are independent of one another.

25. The device of claim 24 wherein the two separate data streams having output sample rates that are not integer multiples of one another.

26. A circuit comprising:

an analog to digital converter clocked at a fixed frequency; and

a loop circuit that receives an output of the analog to digital converter and outputs a sample data stream having a sample rate as a function of a frequency component of a signal received by the circuit.

27. The circuit of claim 26 wherein the signal received by the signal is input to the analog to digital converter.

28. The circuit of claim 26 wherein the circuit comprises a communication circuit.